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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,307	02/10/2004	Ching-Nan Hsiao	10113741	1517

34283 7590 08/24/2005

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EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,307	HSIAO ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *13-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is a first Office action on the merits of Application Serial No. 10/775,307. Currently, claims 1-20 are pending.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-12, drawn to a process of making, classified in class 438, subclass 257.

II. Claims 13-20, drawn to a product, classified in class 257, subclass 314.

3. The inventions are distinct, each from the other because of the following reasons: Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the process as claimed can be used to make other and materially different product. For example, the product as claimed is an NROM. The claimed process can be used to make an EEPROM comprising a vertical floating gate.

4. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Nelson Quintero on 03 August 2005 a provisional election was made with traverse to prosecute the invention of Group I, claims 1-12. Applicant in replying to this Office action must make affirmation of this election. Claims 13-20 have been withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

6. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter that the applicant regards as his invention.

7. Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The phrase "the insulating layer" lacks antecedent basis (claim 1, line 12). The phrase should be replaced with --the conformable oxide layer--.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 2, and 4-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong in view of Acovic et al. (US 5,315,142).

Hong discloses a method for fabricating a multi-bit vertical memory cell (figs. 3-9 and accompanying text). The method comprises: providing a semiconductor substrate 32 having a trench (fig. 6 and col. 3, lines 46-51); forming doped areas S/D, acting as bit lines, in the semiconductor substrate near its surface and the bottom of the trench (fig. 6; col. 2, lines 62-66; and col. 3, lines 52-61); forming bit line insulating layers 46 over each of the doping areas (fig. 7 and col. 3, line 63 – col. 4, line 2); forming a conformable insulating layer 50 over a sidewall of the trench and the bit line insulating layers to locally store electric charge (fig. 9 and col. 4, lines 10-12); and forming a conducting layer 52 over the insulating layer and filling in the trench (fig. 9 and col. 4, lines 13-18).

The method of forming the doping areas comprises: forming a spacer 42 over the sidewall of the trench (fig. 5 and col. 3, lines 38-43); performing ion

implantation in the substrate using the spacer as a mask (fig. 6 and col. 3, lines 52-61); and removing the spacer, as recited in claim 2 (fig. 3 and col. 3, lines 62-63).

The bit line insulating layers 46 are formed by thermal oxidation, as recited in claim 5 (col. 3, lines 63-65).

The thickness of the bit line insulating layers 46 is 300 to 2000 Å, as recited in claim 6 (col. 4, lines 1-2).

A gate dielectric layer 45 is formed between the insulating layer and the trench surface, as recited in claim 9 (fig. 7 and col. 3, lines 65-66).

The gate dielectric layer is a gate oxide layer, as recited in claim 10 (col. 3, lines 65-66).

The conducting layer 52 is a poly layer, as recited in claim 12 (col. 4, lines 13-16).

As explained above, Hong discloses forming a conformable insulating layer 50 over a sidewall of the trench and the bit line insulating layers. While the insulating layer 50 comprises a conformable oxide layer, Hong lacks anticipation of forming a conformable oxide layer over a sidewall of the trench and the bit line insulating layers to locally store electric charge.

On the contrary, the Acovic et al. patent (Acovic) discloses forming a conformable oxide layer over a sidewall of the trench and the bit line insulating layers to locally store electric charge. Acovic discloses a method for forming a memory cell (see figs. 3-12 and accompanying text). The method comprises

forming a conformable insulating layer 115 over the sidewall of a trench (fig. 12 and col. 8, lines 14-23); and forming a conducting layer 40 over the insulating layer and filling in the trench (fig. 12 and col. 8, lines 33-35). Acovic teaches that the conformable insulating layer 115 is either a silicon dioxide-silicon nitride-silicon dioxide layer (ONO), or a silicon rich oxide layer (col.. 8, lines 14-23).

Hong and Acovic are from the same field of endeavor, semiconductor memory devices and methods of fabricating the same. Therefore, the purpose for which Acovic is relied upon would have been recognized in the prior art reference to Hong by one of ordinary skill in the art at the time the invention was made.

The conformable insulating layer 50 in Hong is formed on a floating gate 48', wherein the floating gate is formed of polysilicon (Hong – col. 4, lines 2-7). According to Acovic, an SRO layer is a very good insulator on polysilicon (col. 8, lines 22-23). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Hong by using a conformable oxide layer in place of the conventional ONO layer to locally store electric charge, because an SRO layer is a very good insulator on polysilicon.

As discussed above, Hong discloses forming doped areas in the substrate by performing ion implantation in the substrate. While Hong discloses implanting arsenic ions, Hong lacks anticipation of implanting phosphorus ions, as recited in claim 4. However, it would have been obvious to one of

ordinary skill in the art, at the time the invention was made, to form the doped areas by implanting phosphorus ions in place of arsenic ions because arsenic and phosphorus are art-recognized equivalent N-type dopants commonly used to form N-type doped regions in semiconductor devices.

Acovic does not teach that the thickness of the oxide layer is 50 to 110 Å, as recited in claim 8. However, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Hong and Acovic by forming the oxide layer to a thickness of 50 to 110 Å, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art (see *In re Aller*, 105 USPQ 233).

Hong does not teach that the gate dielectric layer is 50 Å, as recited in claim 11. However, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the gate dielectric layer having a thickness of 50 Å, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art (see *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980)).

9. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffman et al. (5,998,261) in view of Acovic.

The Hoffman et al.. patent (Hoffman) discloses a method for fabricating a multi-bit vertical memory cell (figs. 1-5 and accompanying text). The method comprises: providing a semiconductor substrate 1 having a trench 7 (fig. 2 and

col. 3, lines 51-56); forming doped areas 14a, 14b, acting as bit lines, in the semiconductor substrate near its surface and the bottom of the trench (fig. 3 and col. 4, lines 1-16); forming bit line insulating layers 5, 10 over each of the doping areas (fig. 4; col. 3, lines 38-44; and col. 4, lines 24-26); forming a conformable insulating layer 12 over a sidewall of the trench and the bit line insulating layers to locally store electric charge (fig. 5 and col. 4, lines 51-57); and forming a conducting layer 13 over the insulating layer and filling in the trench (fig. 5 and col. 4, line 58).

The method of forming the doping areas comprises: forming a spacer 8 over the sidewall of the trench (fig. 3; col.. 3, lines 62-67; and col. 4, lines 9-10); performing ion implantation in the substrate using the spacer as a mask (fig. 3 and col. 4, lines 1-8); and removing the spacer, as recited in claim 2 (fig. 4 and col. 4, lines 17-20).

The spacer is silicon nitride, as recited in claim 3 (col. 3, lines 62-67).

The bit line insulating layers 5, 10 are formed by thermal oxidation, as recited in claim 5 (col. 3, lines 38-44 and col. 4, lines 24-30).

The thickness of the bit line insulating layers 5, 10 is 300 to 2000 Å, as recited in claim 6 (col. 3, lines 38-44 and col. 4, lines 24-30).[1]

A gate dielectric layer 10 is formed between the insulating layer and the trench surface, as recited in claim 9 (fig. 4 and col. 4, lines 24-30).

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[1] The thickness of the portions of the oxide layer 10 formed over the doped areas 14a, 14b is 50 nm, which is equivalent to 500 Å.

The gate dielectric layer 10 is a gate oxide layer, as recited in claim 10 (col. 4, lines 24-30).

The conducting layer 13 is a poly layer, as recited in claim 12 (col. 4, line 58).

As explained above, Hoffman discloses forming a conformable insulating layer 12 over a sidewall of the trench and the bit line insulating layers. While the insulating layer 12 comprises a conformable oxide layer, Hoffman lacks anticipation of forming a conformable oxide layer over a sidewall of the trench and the bit line insulating layers to locally store electric charge.

On the contrary, the Acovic et al. patent (Acovic) discloses forming a conformable oxide layer over a sidewall of the trench and the bit line insulating layers to locally store electric charge. Acovic discloses a method for forming a memory cell (see figs. 3-12 and accompanying text). The method comprises forming a conformable insulating layer 115 over the sidewall of a trench (fig. 12 and col. 8, lines 14-23); and forming a conducting layer 40 over the insulating layer and filling in the trench (fig. 12 and col. 8, lines 33-35). Acovic teaches that the conformable insulating layer 115 is either a silicon dioxide-silicon nitride-silicon dioxide layer (ONO), or a silicon rich oxide layer (col.. 8, lines 14-23).

Hoffman and Acovic are from the same field of endeavor, semiconductor memory devices and methods of fabricating the same. Therefore, the purpose for which Acovic is relied upon would have been recognized in the prior art

reference to Hoffman by one of ordinary skill in the art at the time the invention was made.

The conformable insulating layer 12 in Hoffman is formed on a floating gate 11, wherein the floating gate is formed of polysilicon (Hoffman – col. 4, lines 31-34). According to Acovic, an SRO layer is a very good insulator on polysilicon (col. 8, lines 22-23). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Hoffman by using a conformable oxide layer in place of the conventional ONO layer to locally store electric charge, because an SRO layer is a very good insulator on polysilicon.

As discussed above, Hoffman discloses forming doped areas in the substrate by performing ion implantation in the substrate. While Hoffman discloses implanting N-type dopants (col. 3, lines 20-26; col. 4, lines 2-8; and col. 4, lines 13-17), Hoffman lacks anticipation of implanting phosphorus ions, as recited in claim 4. However, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the doped areas by implanting phosphorus ions because phosphorus is an N-type dopant commonly used to form N-type doped regions in semiconductor devices.

Acovic does not teach that the thickness of the oxide layer is 50 to 110 Å, as recited in claim 8. However, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Hoffman and Acovic by forming the oxide layer to a thickness of 50 to 110 Å,

since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art (see *In re Aller*, 105 USPQ 233).

Hoffman does not teach that the gate dielectric layer is 50 Å, as recited in claim 11. However, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the gate dielectric layer having a thickness of 50 Å, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art (see *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
19 August 2005

Mary Wilczewski
Primary Examiner